DC-coupled vertical deflection and East-West output circuit

TDA8350Q

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins
  - short-circuit of the output pins to V_P
- High EMC immunity due to common mode inputs
- Temperature (thermal) protection
- East-West output stage with one single conversion resistor.

GENERAL DESCRIPTION

The TDA8350Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system and an East-West driver for sinking the diode modulator current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_P	quiescent current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
East-West amplifier						
$I_{O(sink)}$	output current (sink only)		–	–	500	mA
$V_{O(sink)}$	peak output voltage	$I_{O(sink)}$ = 10 μA	–	–	40	V
I_{bias}	input bias current		–	–	1	μA
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–65	–	150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8350Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

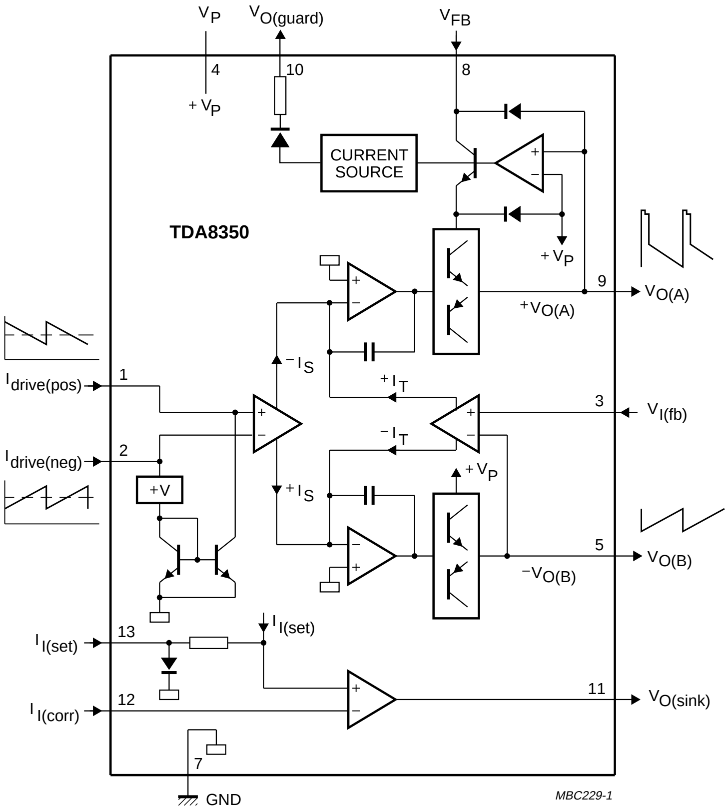


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
$V_{I(fb)}$	3	feedback voltage input
V_P	4	supply voltage
$V_{O(B)}$	5	output voltage B
n.c.	6	not connected
GND	7	ground
V_{FB}	8	flyback supply voltage
$V_{O(A)}$	9	output voltage A
$V_{O(guard)}$	10	guard output voltage
$V_{O(sink)}$	11	East-West amplifier driver (sink) output voltage
$I_{I(corr)}$	12	East-West amplifier input correction current (negative)
$I_{I(set)}$	13	East-West amplifier set input current (positive)

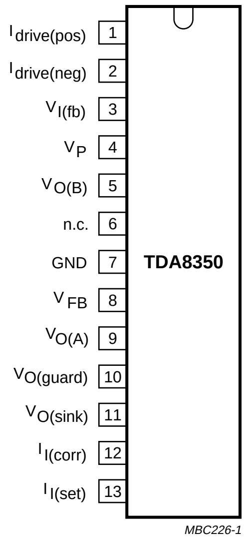


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feed back information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8367 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{(coil)} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 5 and 9)
- short-circuit of the output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during various short-circuit possibilities at the output pins
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

An East-West amplifier is also provided. This amplifier is an inverting amplifier which is current driven with sink current only capabilities.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage	non-operating	–	40	V
			–	25	V
V_{FB}	flyback supply voltage		–	50	V
		note 1		60	V
Vertical circuit					
I_O	output current (peak-to-peak value)	note 2	–	3	A
$V_{O(A)}$	output voltage (pin 9)		–	52	V
		note 1		62	V
Flyback switch					
I_M	peak output current		–	±1.5	A
East-West amplifier					
$V_{O(sink)}$	output voltage	$I_{O(sink)}$ = 10 μA; note 3	–	40	V
$I_{O(sink)}$	output current	$V_{O(sink)}$ = 2 V; note 3	–	500	mA
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–65	150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_{vj}	virtual junction temperature		–	150	°C
$R_{th\ vj\text{-}c}$	resistance v_j-case		–	4	K/W
$R_{th\ vj\text{-}a}$	resistance v_j-ambient in free air		–	40	K/W
t_{sc}	short-circuiting time	note 4	–	1	hr

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. I_O maximum determined by current protection.
3. The operating area is limited by a straight line between the points $V_{O(sink)}$ = 40 V; $I_{O(sink)}$ = 10 μA and $V_{O(sink)}$ = 2 V; $I_{O(sink)}$ = 500 mA.
4. Up to V_p = 18 V.

CHARACTERISTICS

V_P = 17.5 V; V_{FB} = 45 V; $V_{O(sink)}$ = 20 V; f_i = 50 Hz; $I_{I(sb)}$ = 400 μA; T_{amb} = 25°C; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		9	–	25	V
V_{FB}	flyback supply voltage		V_p	–	50	V
		note 1	–	–	60	V
I_P	supply current	no signal; no load	–	30	55	mA
Vertical circuit						
V_O	output voltage swing (scan)	I_{diff} = 0.6 mA (p-p); V_{diff} = 1.8 V (p-p); I_O = 3 A (p-p)	19.8	–	–	V
LE	linearity error	I_O = 3 A (p-p);	–	1	2	%
		I_O = 50 mA (p-p); note 2	–	1	2	%
V_O	output voltage swing (flyback) $V_{O(A)}$ - $V_{O(B)}$	I_{diff} = 0.3 mA; I_O = 1.5 A (M)	–	39	–	V
V_{DF}	forward voltage of the internal efficiency diode ($V_{O(A)}$ - V_{FB})	I_O = –1.5 A (M); I_{diff} = 0.3 mA	–	–	1.5	V
$\|I_{os}\|$	output offset current	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	30	mA
$\|V_{os}\|$	offset voltage at the input of the feedback amplifier $V_{I(fb)}$ - $V_{O(B)}$	I_{diff} = 0; $I_{I(sb)}$ = 50 to 500 μA	–	–	18	mV
$\Delta V_{os}T$	output offset voltage as a function of temperature	I_{diff} = 0;	–	–	72	μV/K
$V_{O(A)}$	DC output voltage	I_{diff} = 0; note 3	–	8	–	V
G_v	open loop voltage gain (V_{9-5}/V_{1-2})	notes 4 and 5	–	80	–	dB
	open loop voltage gain (V_{9-5}/V_{3-5}; V_{1-2} = 0)	note 4	–	80	–	dB
V_R	voltage ratio V_{1-2}/V_{3-5}		–	0	–	dB
f_{res}	frequency response (–3 dB)	note 6	–	40	–	Hz
G_I	current gain (I_O/I_{diff})		–	5000	–	
ΔG_IT	current gain drift as a function of temperature		–	–	10^{-4}	/K
$I_{I(sb)}$	signal bias current		50	400	500	μA
I_{FB}	flyback supply current	during scan	–	–	100	μA
PSRR	power supply ripple rejection	note 7	–	80	–	dB
$V_{I(DC)}$	DC voltage at the input		–	2.7	–	V
$V_{I(CM)}$	common mode input voltage	$I_{I(sb)}$ = 0	0	–	1.6	V
I_{bias}	input bias current	$I_{I(sb)}$ = 0	–	0.1	0.5	μA
$I_{O(CM)}$	common mode output current	$\Delta I_{I(sb)}$ = 300 μA (p-p); f_i = 50 Hz; I_{diff} = 0	–	0.2	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
East-West amplifier						
$V_{O(sink)}$	saturation voltage	$I_{O(sink)}$ = 500 mA; $I_{I(corr)}$ = 0 μA; note 8	–	2.0	2.5	V
G_v	open loop voltage gain (V_{11}/V_{12})		–	47	–	dB
f_{res}	frequency response (–3 dB)		–	4000	–	Hz
LE	linearity error	$V_{O(sink)}$ = 3 V	–	–	1	%
		$V_{O(sink)}$ = 10 V; note 2	–	–	0.5	%
I_{bias}	input bias current (pin 12)		–	–	2	μA
$V_{I(DC)}$	DC input voltage		–	1	–	V
I_{set}	offset voltage set current		–	1	–	mA
V_{13-7}	maximum allowed voltage at pin 13		–	–	0.3	V
Guard circuit						
I_O	output current	not active; $V_{O(guard)}$ = 0 V	–	–	50	μA
	output current	active; $V_{O(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{O(guard)}$	output voltage	I_O = 100 μA	–	–	5.5	V
	allowable voltage on pin 10	maximum leakage current = 10 μA	–	–	40	V

Notes

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 8 and pin 4. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.5).
2. The linearity error is measured without S-correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal I_5 - I_9 (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below;
   $$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}}\ ;\ NAB = \frac{a_{max} - a_{min}}{a_{avg}}$$
3. Referenced to V_P.
4. V values within formulae, relate to voltages at or between relative pin numbers, i.e. V_{9-5}/V_{1-2} = voltage value across pins 9 and 5 divided by voltage value across pins 1 and 2.
5. V_{3-5} AC short-circuited.
6. Frequency response V_{9-5}/V_{3-5} is equal to frequency response V_{9-5}/V_{1-2}.
7. At $V_{(ripple)}$ = 500 mV eff; measured across R_M; f_i = 50 Hz.
8. The output pin 11 requires a capacitor of minimum value 68 nF.

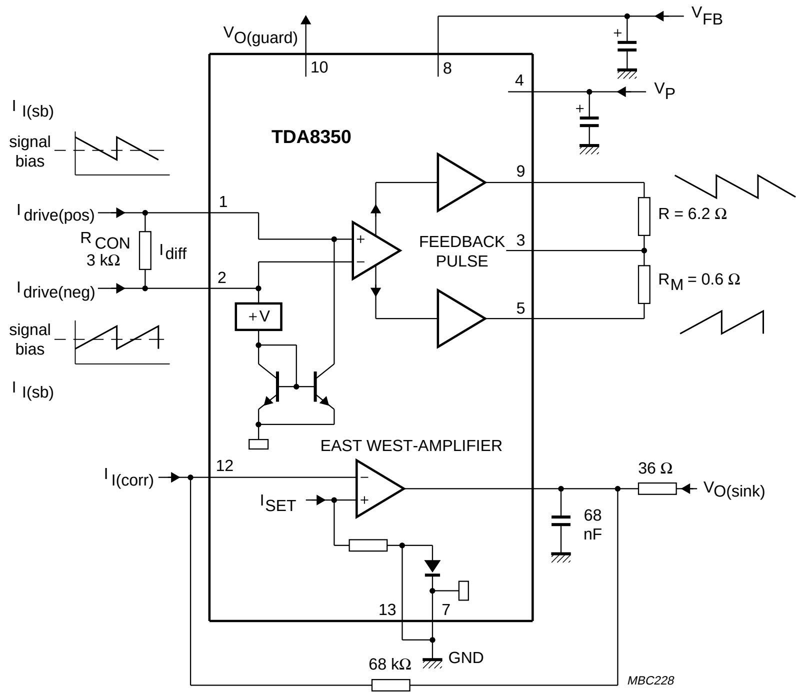
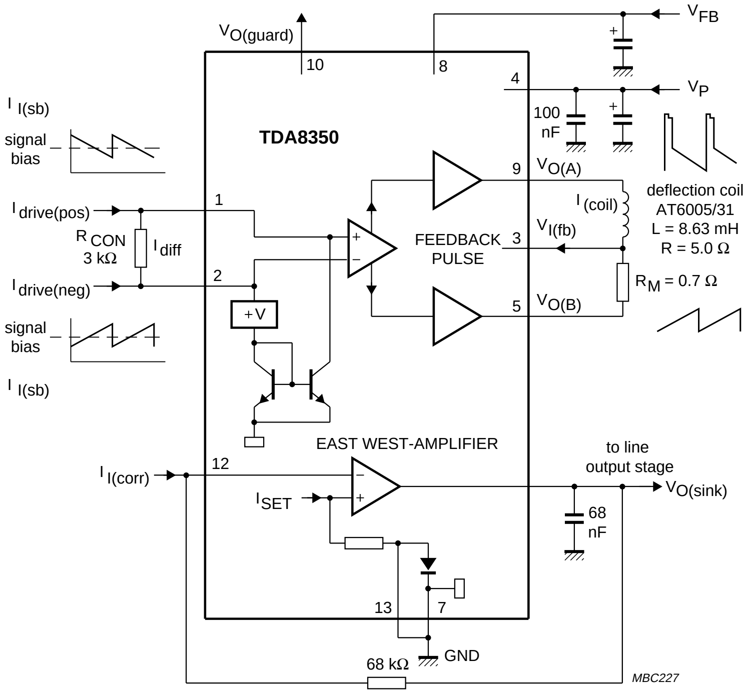


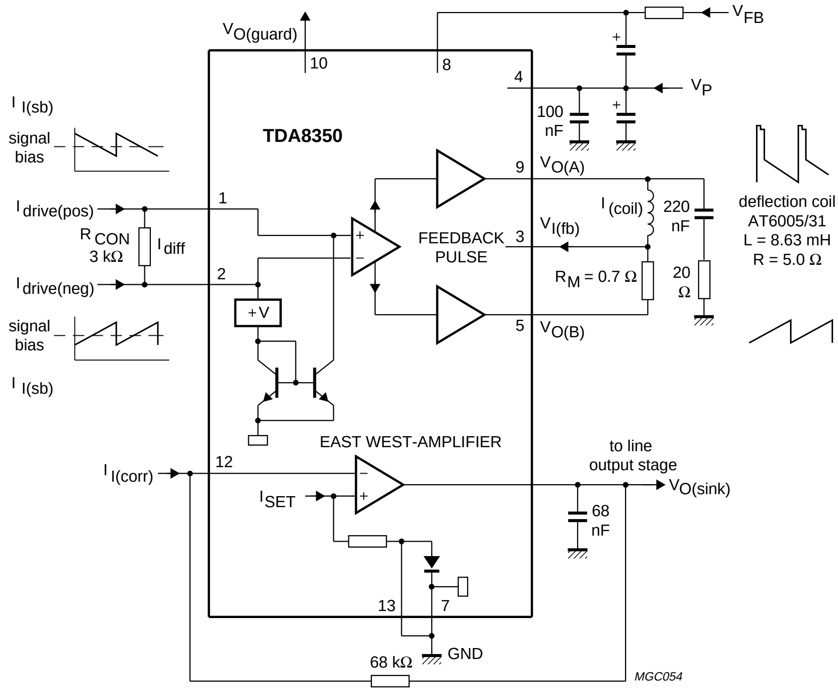
Fig.3 Test circuit.

APPLICATION INFORMATION



V_P = 14 V; $I_{O(p\text{-}p)}$ = 2.14 A; $I_{I(sb)}$ = 400 μA; $I_{diff(p\text{-}p)}$ = 500 μA; V_{FB} = 42 V; t_{FB} = 0.6 ms.

Fig.4 Application diagram.



V_P = 14 V; $I_{O(p-p)}$ = 2.14 A; $I_{I(sb)}$ = 400 µA; $I_{diff(p-p)}$ = 500 µA; V_{FB} = 60 V; t_{FB} = 0.4 ms.

Fig.5 Application circuit; 50 V ≥ V_{FB} ≥ 60 V.